Course Code: ECE 7103

Advanced Digital Design

Credit Hours: 3

Instructor: Dr. Shoab A. Khan
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TA: Ali Jabir

Text Books

Digital Design of Signal Processing Systems: A Practical Approach by Shoab Khan Feb 2011, John Wiley & Sons

References

1. VLSI Digital Signal Processing Systems, Design and Implementation by Keshab K Parhi
2. Verilog HDL-A guide to digital design and synthesis by Samir Palnitkar, Prentice Hall Publisher
3. Advanced Digital Design With Verilog HDL by Ciletti, Michael D

Goals This course is designed to introduce engineers and designers advanced digital design concepts. The students are taught a spectrum of techniques for designing and mapping of algorithms on FPGAs / ASICS using HDLs.

Pre-requisites by Topics

Digital Logic Design, Computer Architecture, Signals and Systems/Digital Signal Processing,

Objectives

The objective of the course is to teach students

1. Verilog as hardware description language
2. FPGA architecture and logic Synthesis concepts
3. Architecture of basic building blocks, adders, multipliers, shifters
4. Converting floating-point algorithms design in Matlab to Fixed-point format
5. Effective HW mapping techniques: Fully parallel, Unfolded, Folded and Time-shared, micro-coded architectures
6. Designing State-machines based architecture

Pre-requisites by Topics

Digital Logic Design, Computer Architecture, Signals and Systems,

Topics

1. High-level digital design methodology using Verilog, Design, Implementation, and Verification,
    a. Introduction of SystemVerilog and SystemC
2. Application requiring HW implementation, Floating-Point to Fixed-Point Conversion
3. Options for top-level design
    a. KPN based design
    b. Network on Chip
4. FPGA Architectures
    a. Embedded Blocks, Multipliers, Adders, Carry Chains
    b. Embedded Processors, and interfaces
    c. System generator
    d. Logic Synthesis
5. Architectures for Basic Building Blocks, Adder, Compression Trees, and Multipliers, Barrel Shifter
6. Dedicated Fully Parallel Architecture
7. Transformations for high speed
    a. Pipelining
    b. Retiming
    c. C-Slow Retiming
    d. Look-ahead transformation
    e. Parallel processing
8. Optimized Time shared Architecture
    a. Folding transformation
9. Hardwired State Machine based Design
10. Micro Program State Machine based Design

Computer Usage

Verilog Simulator, FPGA Logic Synthesis tools

Grading Criteria

Quizzes 5% ,
Labs & assignments to be developed ALONE: 10-15%,
Final project, teams of 1-3 students: 10-15%,
One/Two sessionals: 25-30%,
Final: 35-50